**Stratix 10**

**Definitions:**

**Stratix 10 GT FPGAs**: For the most demanding applications requiring ultra-high bandwidth and performance Stratix 10 GT FPGA transceivers support data rates up to 56 Gbps.

**Stratix 10 GX FPGAs**: Built for high performance and bandwidth applications such as multi-100G/400G systems Stratix 10 GX FPGA transceivers support 32 Gbps chip-module, chip-to-chip, and backplane operations at up to 28 Gbps Built for high performance and power-efficient computing applications such as data center acceleration, radar, and line card processing.

**Stratix 10 SX SoCs**: Built for maximum processor performance per watt for high-bandwidth applications with an integrated HPS Stratix 10 SX SoCs feature hard processor system with 64 bit quad-core ARM Cortex-A53 processor

**Key Points:**

* Stratix 10 FPGAs offer advanced performance in bandwidth and system integration. Includes hard processor systems which can provide the highest performance in the industry and most power-efficient FPGAs and SoCs.
* Hyperflex architecture (manufactured on Intel 14 nm Tri-Gate process, powering immense levels of performance, when coupled with 64 bit quad core ARM Cortex A53 processors and advanced heterogeneous development and debug tools, this device offers the most versatile heterogeneous computing platform.

**Differentiating Features & Performance Topics:**

* HyperFlex Architecture, 2 times the core performance of prior generation high-performance FPGAs
* 10 TFLOPs of single-precision floating-point DSP performance, 4 times the processor data throughout prior generation SoCs
* >2.5 tbps bandwidth for serial memory, support Hybrid Memory Cube; >1.3 Tbps bandwidth for parallel memory interfaces
* Largest monolithic FPGA device w/ > 4M logic elements
* 70% lower power usage than prior generations
* 64 bit quad core ARM Cortex A53 process optimized for ultra-performance per watt
* Heterogeneous debug, profiling, and whole chips visualization
* Fastest compile times in industry, C-based design entry using Altera SDK for OpenCL, offering a design environment that’s easy to implement on FPGAs
* Smaller footprint, higher reliability, lower system power, faster time to power FPGAs and SoCs

**Stratix V**

**Definitions:**

* **Stratix V GX FPGAs** with transceivers: Integrate up to 66 full-duplex, 14.1 Gbps transceivers and up to 6 x72 bit DIMM DDR3 memory interfaces supporting 933 MHz
* **Stratix V GS FPGAs** with enhanced digital signal processing (DSP) capabilities and transceivers: Integrate up to 3,926 18x18, high-performance, variable-precision multipliers, 48 full-duplex, 14.1 Gbps transceivers, and up to 6 x72 bit DIMM DDR3 memory interfaces supporting 933 MHz
* **Stratix V GT FPGAs** with transceivers: Integrate four 28 Gbps transceivers and 32 full-duplex, 12.5 Gbps transceivers with up to 4 x72 bit DIMM DDR3 memory interfaces supporting 933 MHz
* **Stratix V E FPGAs:** Up to 950K logic elements (LEs), 52-megabit (Mb) RAM, 704 18x18 high-performance, variable-precision multipliers, and 840 I/Os

**Key Points:**

* Altera's [28 nm Stratix® V FPGAs](https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/wp/wp-01125-stxv-28nm-innovation.pdf) deliver the industry's highest bandwidth, highest level of system integration, and ultimate flexibility with reduced cost and the lowest total power for high-end applications.

**Differentiating Features & Performance Topics:**

* Breakthrough Bandwidth w/ Power Efficient Transceivers: Integrated 28.05 and 14.1 Gbps transceivers, with up to 50 percent lower transceiver power compared to previous-generation devices.
* 6 x 72 DDR3 memory interfaces at 933 MHz
* 2.5 TMACS of signal processing performance
* PCI Express Gen3, Gen2, Gen1 hard intellectual property
* Integrated hard IP in core and transceivers, which harden critical datapath components to eliminate system bottlenecks
* Deliver up 14.3M ASIC gates, up 1.19M logic elements
* Partial reconfig. Saving board space, cost, power
* Increased clocking flexibility and replace on-board voltage-controlled crystal oscillator
* EDC , no need external PHY interface optical modules
* Change core functionality on fly
* Support multiple protocols, CvP: less complex board design
* PPT, maximizes core performance, reduces power

**Arria 10**

**Definitions:**

Arria 10  delivers the highest performance at 20 nm. Arria 10 FPGAs and SoCs are up to 40 percent lower power than previous generation FPGAs and SoCs and feature the industry’s only hard floating-point digital signal processing (DSP) blocks with speeds up to 1,500 giga floating-point operations per second (GFLOPs).

**Key Points:**

* One grade faster
* [The industry’s only midrange 28.3 Gbps support](https://www.altera.com/products/fpga/features/transceivers/arr10-transceivers.html)
* Highest performance 2,666 Mbps DDR4 SDRAM memory interface
* IEEE 754-compliant hard floating-point with 1,500 GFLOPS of DSP performance
* 96 transceiver lanes deliver 3.6 Tbps of serial bandwidth

**Differentiating Features & Performance Topics:**

* Programmable Power Tech- Reduce device power in lower performance circuits, still highest performance
* Smart Voltage ID, optimum lower voltage
* VCC power Manager- operates devices multiple voltage levels for either higher performance or lower power
* Lower static power grades – Select devices w/ lower maximum static power

**Arria V**

**Definitions:**

Arria V offers highest bandwidth and the lowest total power for midrange applications. I.e. Remote radio units, 10G/40G line cards, and broadcast studio equipment.

**Key Points:**

* Offers a number of solutions to meet bandwidth requirements of your application while balancing power and cost targets

**Differentiating Features & Performance Topics:**

* Lowest power per bandwidth for midrange applications
* Ideal for power-sensitive designs that require transceivers up to 12.5 Gbps.
* 10G data rates, Arria V GZ FPGAs consume less than 180 mW per channel and 12.5 Gbps consume less than 200mW per channel
* Deliver lowest static power
* For speeds up to 10.3125 Gbps and providing superior fabric with hard IP designed to lower dynamic power
* Provides 40% on average power reduction compared to previous generation of midrange FPGAs
* Reduce system power, cost and board space by integrating hard processor, consisting of processors, peripherals, and memory controllers

**Cyclone V**

**Definitions:**

Cyclone V FPGAs provide the industry’s lowest system cost and power. Along with performance levels that make device family ideal for differentiating your high volume applications.

**Key Points & Definitions:**

* Up to 40% lower total power compared with previous generation, efficient logic integration capabilities, integrated transceiver variants, SOC FPGA variants w/ ARM- based hard processor system (HPS)

**Differentiating Features & Performance Topics:**

* Optimized for lowest system cost and power for a wide spectrum of general logic and DSP applications
* Optimized for lowest cost and power for 614 Mbps to 3.125 Gbps transceiver applications
* FPGA industry’s lowest cost and power for 6.144 Gbps transceiver applications
* Reduce system power, system cost, and board space by integrating HPS consisting of processors, peripherals, and memory controller w/ FPGA fabric using high bandwidth interconnect backbone
* Integrate abundance of hard IP blocks
* Shortens overall system cost, power, and design time.
* Key hard IP blocks:
  + Hard memory controllers supporting MHz DDR3 SDRAM w/ optional ECC (Error Correction Code) support
  + PCI Express Gen2 w/ multifunction support
  + Variable precision digital signal processing blocks
  + HPS Dual core ARM Cortex A9 MPCore processor

**Max 10**

**Definitions:**

Altera MAX 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, single chip small form factor programmable logic device. Built upon single chip heritage, densities range from 2K-50K Les, using either single or dual-core voltage supplies. The MAX 10 family has both small wafer scale packaging (3mm x 3mm) and high I/O pin count packaging offering.

**Key Points:**

* Built on TSMC 55 nm embedded NOR flash technology, enabling instant-on functionality. Integrated features include analog-to-digital converters (ADCs) and dual configuration flash allowing to store and dynamically switch between two images on a single chip.

**Differentiating Features & Performance Topics:**

* Dual configuration flash- Single, on-die flash memory supports dual configuration, for true fail-safe upgrades with thousands of possible reprogram cycles.
* Analog blocks- Integrated analog blocks with ADCs and temperature sensors provide lower latency and reduced board space with more flexible sample sequencing
* Instant on- Max 10 FPGAs can be first usable on system board to control bring-up of other components such as high density FPGAs, ASICs, ASSPs, and processors
* Nios soft core embedded processor- MAX 10 FPGAs support the integration of Altera’s soft core Nios II embedded processors, providing embedded developers a single-chip, fully configurable, instant-on processor subsystems
* DSP blocks – ideal for high performance, high precision applications using integrated 18x18 multipliers
* DDR3 external memory interfaces – MAX 10 FPGAs support DDR3 SDRAM and LPDDR2 interfaces
* User flash – With up to 736 KB on-die user flash code storage, MAX 10 FPGAs enable advanced single chips Nios II embedded applications. The amount of user flash depends on configuration options

**Max V**

**Definitions:**

Max V CPLDs deliver the market’s best value. Featuring a unique, non-volatile architecture, MAX V devices provide new features up to 50% lower total power compared to competitive CPLDs.

**Key Points:**

* Offers a number of solutions to meet bandwidth requirements of your application while balancing power and cost targets. Up to 50% lower total power vs. other equivalent-density CPLDs on the market

**Differentiating Features & Performance Topics:**

* Extended battery life with static power as low as 45 uW
* As few as one power supply (Vcc-core) required, which also lowers bill of materials (BOM) costs
* In-system programming (ISP), which lets you program the device while it is in operation, so you can perform in-field updates without affecting overall system operation
* User flash memory, embedded flash memory that provides non-volatile memory storage of critical system information
* Digital PLLs (DPLLs), which enable flexible implementation of designs requiring frequency multiplication or phase shifting

**PowerSoC**

**Definitions:**

With the integrated Enpirion PowerSoCs, we get an industry-leading combination of small footprint, low noise performance, and high efficiency, in qualified and reliable solutions that enable you to complete your design faster.

**Differentiating Features & Performance Topics:**

* Over temperature protector
* Pin compatible
* Resistor divider

**Nios II Processor**

**Definitions:**

The Nios II processor is the world’s most versatile processor and most widely used. The process delivers unprecedented flexibility for cost-sensitive, real-time, safety-critical, ASIC-optimized, and applications processing needs. The Nios processor supports all Altera SoC and FPGA families.

**Key Points:**

* Power and cost sensitive
* Real time
* Applications processing
* Safety critical

**Differentiating Features & Performance Topics:**

* Nios II economy processor core is ideal for microcontroller applications. The Nios II economy processor core, software tools, and device drivers are offered free of charge.
* Absolutely deterministic, jitter free real-time performance with unique hardware real-time features
  + Vector Interrupt Controller
  + Tightly Coupled Memory
  + Custom instructions (ability to use FPGA hardware to accelerate a function)
  + Supported by industry-leading Real-Time Operating Systems
  + Nios II processor is the ideal real-time processor to use with DSP Builder-based hardware accelerators to provide deterministic, high performance real-time results
* With a simple configuration option, the Nios II fast processor core can use a memory management unit (MMU) to run embedded Linux. Both open source and commercially supported versions of Linux for Nios II are available.
* Certify your design for DO-254 compliance by using Nios II Safety Critical processor core along with the DO-254 compliance design service offered by HCell.

**Intellectual Property**

**Definitions:**

Altera IP portfolio includes a unique combination of soft and hard IP cores, along with reference designs to complement performance and IP strategies. You can evaluate our IP using our no-hassle licensing features, and verify functionality and performance on hardware.

**Key Points:**

* IP Cores
* Reference Designs
* Silicon
* IP Partners
* OpenCore Plus
* Development Kits
* Design Software

**Differentiating Features & Performance Topics:**

* Altera offers the 10GbE MegaCore function intellectual property (IP) core for building system with Ethernet connection ranging from 10M to 10G.
* Single Speed 10Gb operations as well as 1G/10GbE and 10/100M/1G/10GbE multi speed options which allow you to build a flexible Ethernet port to connect to 10GbE or multiple-data rate 10/100/1000MbE or 1G/10GbE external devices, optical modules or copper PHY devices or directly to a copper backplane
* 40 Gbps Ethernet and 100 Gbps Ethernet (100GbE) MegaCore function intellectual property (IP) cores for building system with high throughout-rate standard Ethernet connections.
* Interlaken is a scalable protocol that enables chip-to-chip packet transfers at rates from 10 Gbps to 100 Gbps and beyond. Continues to scales with today’s demand for more bandwidth and high performance needs. Interlaken IP Core includes leading transceivers, physical medium attachment, physical coding sublayer (PCS), and media access control (MAC) layers. Saves 30% to 50% of FPGA logic resources.
* Parameters tuning enables bandwidth usage improvement as high as 35%, 15% IP core timing margin accelerates full design closure
* Consistent delivery of over 150 million packets / second on multiple customer platforms and across various vertical markets. High frequency user clocking performance
* PCI Express is a high performance, scalable, and feature-rich serial protocol w/ data transfer rates from 2.5 GT/s to 8.0 GT/s. Includes hardened protocol stack, which includes the transaction and data link layers, and hardened physical layers, which include both the physical coding sublayer and physical medium attachment.

**External Memory Interfaces:**

* Introducing the [Hybrid Memory Cube (HMC) MegaCore](https://www.altera.com/solutions/technology/serial-memory/hybrid-memory-cubes.html) providing the highest performances for emerging, rapidly increasing memory bandwidth applications.
* Hardware-verified support for DDR3/4 features in Arria® 10 device:
* PHY-only, error correction code (ECC), 144 bit, multirank (dual-rank, quad-rank)
* Ping-Pong PHY
* X4 DQ/DQS
* DDR4 RDIMM
* EMIF Debug Toolkit and On-chip EMIF Debug Toolkit
* Hardware-verified support for QDR IV up to 800 MHz
* DDR3/3L, DDR2, LPDDR2 hardware support in MAX® 10 FPGAs
* Power saving enhancement in MAX 10 FPGAs
* During self refresh, tri-state A/C pins and disable all DDR input buffers except CKE and RESET

**Development Kits**

**Definitions:**

Altera development kits provide high-quality design environment for engineers. A wide variety of kits help simplify the design and process and reduce time to market. Development kits include software, reference designs, cables, and programming hardware.

**Key Points:**

* Stratix V Kits
* Stratix IV Kits
* Stratix III Kits
* Stratix II Kits

**Quartus II Software**

**Key Points:**

* Altera SDK OpenCL
* Qsys system integration tool
* DSP Builder Advanced Blockset
* System Console
* Transceiver Toolkit
* External Memory Interface Toolkit
* TimeQuest timing analyzer
* PowerPlay power analysis tools
* Fused datapath
* Multiprocessor support
* Incremental compile
* Design entry and synthesis
* Verification and board level tools
* Design Optimization

**Differentiating Features & Performance Topics:**

* OpenCL – C based language
* Qsys- interconnect logic to connect IP and subsystems
* DSP, simulate system implementation
* System level debug tool, system console, real time to read and write transcations
* Transceiver Toolkit is based on System Console. This toolkit gives you real-time access to your transceiver settings, visualizes the signal eye, and quickly performs transceiver link verification
* External Memory Interface Toolkit is based on System Console. Identifying calibration issues
* Numerous optimization features to enhance design process
* Timing analyzer
* Reduce compilation by 70%

**Altera SDK OpenCL**

**Definitions:**

The OpenCL standard is the first open, royalty-free, unified programming model for accelerating algorithms on heterogeneous systems. OpenCL allows the use of a C-based programming language for developing code across different platforms such as central processing units (CPUs), graphic processing units (GPUs), digital signal processors (DSPs), and field-programmable gate arrays (FPGAs).

**Key Points:**

* An emulator to step through the code on an x86 and ensure it is functionally correct
* A detailed optimization report to understand the load and store inner loop dependencies
* An OpenCL compiler capable of performing over 300 optimizations on the kernel code and producing the entire FPGA image in one step